

AMENDMENTS TO THE CLAIMS

Listing of the Claims:

1. (Canceled)
2. (Canceled)
3. (Previously presented) A thin film transistor array panel for an X-ray detector, the thin film transistor array panel comprising:
 - a gate wire formed on an insulating substrate and comprising a gate line and a gate electrode connected to the gate line;
 - a gate insulating layer formed on the gate wire;
 - a semiconductor layer formed on the gate insulating layer;
 - a data wire formed on the gate insulating layer and comprising:
 - a data line which intersects the gate line;
 - a source electrode connected to the data line and disposed on the semiconductor layer; and
 - a drain electrode disposed on the semiconductor layer separate from the source electrode;
 - a photo diode comprising:
 - a first electrode connected to the drain electrode;
 - a second electrode which faces the first electrode; and

a photo-conductive layer disposed between the first electrode and the second electrode;

a passivation layer disposed on the photodiode, the semiconductor layer, the data wire and the drain electrode, the passivation layer having a contact hole which exposes the second electrode; and

a bias signal line disposed directly on the passivation layer, connected to the second electrode through the contact hole and comprising a light blocking layer which covers the photo diode.

4. (Previously presented) The thin film transistor array panel of claim 3, wherein the photo-conductive layer comprises a first amorphous silicon film comprising an N type impurity, a second amorphous silicon film disposed on the first amorphous silicon film and comprising intrinsic amorphous silicon, and a third amorphous silicon film disposed on the second amorphous silicon film and comprising a P type impurity.

5. (Previously presented) A thin film transistor array panel for an X-ray detector, the thin film transistor array panel comprising:

a gate wire formed on an insulating substrate and comprising a gate line and a gate electrode connected to the gate line;

a gate insulating layer formed on the gate wire;

a semiconductor layer formed on the gate insulating layer;

a data wire formed on the gate insulating layer and comprising:

a data line which intersects the gate line;

a source electrode connected to the data line and disposed on the semiconductor layer; and

a drain electrode disposed on the semiconductor layer separate from the source electrode;

a photo diode comprising:

a first electrode connected to the drain electrode;

a second electrode which faces the first electrode; and

a photo-conductive layer disposed between the first electrode and the second electrode; and

a bias signal line connected to the second electrode, wherein

the semiconductor layer is disconnected in a region disposed between the source electrode and the drain electrode, and

the region disposed between the source electrode and the drain electrode is absent semiconductor material to transmit a signal to the data line.

6. (Previously presented) The thin film transistor array panel of claim 5, wherein the photo-conductive layer comprises a first amorphous silicon film comprising an N type impurity, a second amorphous silicon film disposed on the first amorphous silicon film and comprising intrinsic amorphous silicon, and a third amorphous silicon film disposed on the second amorphous silicon film and

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comprising a P type impurity.